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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,844	09/25/2003	**Sujat Jamil**	MP1491	8695

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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/671,844	JAMIL ET AL.	
	Examiner	Art Unit	
	ROBERT E. FENNEMA	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 June 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-36 have been considered. Claims 32-36 added as per Applicant's request. Claims 1, 3, 8, 11, 13, 16, 18, and 31 amended as per Applicant's request.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-9, 11-19 and 21-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Merchant et al. (US Patent 6,385,715, herein Merchant).

4. As per claim 1, Merchant teaches a method comprising:

issuing an instruction selected from a queue (Column 3, Lines 25-33; Column 3, Lines 43-47);

enqueuing the instruction issued within a recirculation queue in one of a blocked state and an unblocked state if completion of the instruction is prevented by a detected blocking condition (Column 8, Lines 42-53); and

reissuing the instruction from the recirculation queue if a detected blocking condition of at least one instruction within the recirculation queue, other than the

instruction, is satisfied (Column 8, Lines 42-53. Also see Column 11, Lines 19-22, when one instruction can go in the queue, all instructions may be unloaded).

5. As per claim 2, Merchant teaches: The method of claim 1, wherein issuing comprises:

arbitrating between a plurality of queues to select a queue (Column 9, Lines 42-52);

selecting a current instruction from the queue selected (Column 9, Lines 42-52); and

issuing the current instruction for the queue selected (Column 9, Lines 42-52).

6. As per claim 3, Merchant teaches the method of claim 2, wherein issuing the current instruction comprises:

determining a state of the current instruction (Column 9, Lines 58-64);

selecting an alternate queue from the plurality of queues if a state of the instruction is blocked (Column 9, Lines 65-67); and

issuing an instruction selected from the alternate selected queue (Column 9, Lines 42-55).

7. As per claim 4, Merchant teaches the method of claim 1, wherein enqueuing comprises:

detecting the blocking condition prohibiting the instruction issued from completion

(Column 8, Lines 54-67);

placing the instruction within the recirculation queue (Column 9, Lines 1-8); setting a state of the instruction as blocked to prohibit reissue of the instruction (Column 9, Lines 25-33) (All instructions in the replay queue are blocked and will not be not be reissued until the blocking condition has been cleared.); and

storing the detected blocking condition (Column 12, Lines 51-57) (The fact that the replay unloading controller can selectively choose which long latency instruction is referenced by data return signal shows that the blocking condition was stored.).

8. As per claim 5, Merchant teaches the method of claim 1, further comprising:

identifying blocking conditions of instructions within the recirculation queue (Column 12, Lines 51-57);

determining whether any blocking condition of any instruction within the recirculation queue is satisfied (Column 12, Lines 51-57);

enabling recirculation of instructions from the recirculation queue by setting a state of each instruction within the recirculation queue to an unblocked state if any blocking condition is satisfied (Column 12, Lines 58-60).

9. As per claim 6, Merchant teaches the method of claim 1, wherein reissuing instructions comprises:

receiving a request to issue an instruction contained within the recirculation queue (Column 12, Lines 51-55) (The data return signal is a request to issue since

instructions are issued based on the receiving of data.);

determining a state of a current instruction of the recirculation queue (Column 12, Lines 55-57);

issuing the current instruction if the state of the current instruction is an unblocked state in response to the received request (Column 12, Lines 57-60; Column 12, Lines 14-21); and

disregarding the request if the state of the current instruction is a blocked state (Column 12, Lines 57-60; Column 12, Lines 14-21) (The unloading controller chooses which of the replay queues should be unloaded based on the data return signal based on the control signals to the mux, the instruction is either issued if it was the instruction chosen by the unloading controller or denied if it was not chosen.).

10. As per claim 7, Merchant teaches the method of claim 1, wherein enqueuing comprises:

determining whether the detected blocking condition preventing the instruction issued from completion is a transient blocking condition (Column 9, Lines 1-4; Column 7, Lines 1-9. Placing instructions in the replay loop is a determination of a transient blocking condition since it is timed sensitive condition based on an L0 cache miss, L1 hit. The loop is designed to provide enough time for the data to be there by the time the instruction is reissued.);

setting a state of the instruction to an unblocked state if the detected blocking condition is transient (Column 8, Lines 65-67; Column 9, Lines 1-8. As was discussed

above, instructions are only in a blocked state if they are put in the replay queue. Since transient instructions are put in the replay loop, they are not blocked and ready for issue as soon as they arrive at the mux); and

resetting a state of each instruction within the recirculation queue to an unblocked state (Column 9, Lines 28-36).

11. As per claim 8, Merchant teaches the method of claim 1, wherein reissuing the instructions comprises:

issuing an unblocked instruction in response to a received request (Column 9, Lines 28-36},

enqueuing the reissued instruction if a blocking condition of the instruction remains unsatisfied (Column 7, Lines 9-12);

setting a state of the reissued instruction to a blocked state (Column 8, Lines 42-53); and

storing the blocking condition (Column 12, Lines 51-57. The fact that the replay unloading controller can selectively choose which long latency instruction is referenced by data return signal shows that the blocking condition was stored.).

12. As per claim 9, Merchant teaches the method of claim 1, wherein the detected blocking condition is one of a data blocking condition and a resource blocking condition (Column 8, Lines 13-16).

13. Claims 11-19 are substantially similar to Claims 1-9, and are rejected for the same reasons.

14. As per claim 21, Merchant teaches: An apparatus, comprising:

a received instruction queue to store received instructions (Column 3, Lines 25-33; Column 3, Lines 43-47);

a recirculation queue (Figure 1, the combination of loop 156 and queue 170, starting at controller 154); arbitration logic to select one of the received instruction queue and the recirculation queue from which to issue a current instruction (Column 9, Lines 42-52); and

blocked instruction detection logic to identify instructions blocked from execution by detected blocking conditions, and to enqueue the instructions onto the recirculation queue in one of a blocked state and an unblocked state, including a respective blocking condition of each instruction within the recirculation queue, wherein instructions having a transient blocking condition are enqueued onto the recirculation queue in the unblocked state (Column 9, Lines 1-8).

15. As per claim 22, Merchant teaches: The apparatus of claim 21, wherein the blocked instruction detect logic further comprises:

blocked condition satisfaction logic to detect whether a blocking condition of an instruction within the recirculation queue is satisfied and to set a state of each

instruction within the recirculation queue to an unblocked state if a blocking condition of an instruction within the recirculation queue is satisfied (Column 9, Lines 25-36).

16. As per claim 23, Merchant teaches: The apparatus of claim 21, wherein the arbitration logic to determine a state of a selected instruction, select the received instruction queue if a state of the selected instruction is blocked, and issue an instruction selected from the received instruction queue (Column 9, Lines 64-67).

17. As per claim 24, Merchant teaches: The apparatus of claim 21, wherein the blocked instruction detect logic to determine whether the detected blocking condition is a transient blocking condition (Column 9, Lines 1-4; Column 7, Lines 1-9) (Placing instructions in the replay loop is a determination of a transient blocking condition since it is timed sensitive condition based on an L0 cache miss, L1 hit. The loop is designed to provide enough time for the data to be there by the time the instruction is reissued.), set a state of the instruction placed within the queue to an unblocked state if the detected blocking condition is transient (Column 8, Lines 65-67; Column 9, Lines 1-8), and reset a state of each instruction within the recirculation queue to an unblocked state to enable reissue of instructions contained within the recirculation queue (Column 9, Lines 28-36).

18. As per claim 25, Merchant teaches: The apparatus of claim 21, wherein the blocked instruction detect logic to enqueue a reissued instruction if a blocking condition of the instruction remains unsatisfied (Column 7, Lines 9-12), to set a state of the

reissued instruction to a blocked state (Column 8, Lines 42-53) and to store the blocking condition (Column 12, Lines 51-57) (The fact that the replay unloading controller can selectively choose which long latency instruction is referenced by data return signal shows that the blocking condition was stored.).

19. As per claim 26, Merchant teaches: A system comprising:

a memory controller coupled to a memory (Column 4, Lines 20-23);

a processor coupled to the memory via a bus (Figure 1, item 100), the processor including:

a bus interface unit coupling an execution core to a cache memory including:

a received instruction queue to store received instructions (Column 3, Lines 25-33),

a recirculation queue (Figure 1, the combination of loop 156 and queue 170, starting at controller 154), arbitration logic to select one of the received instruction queue and the recirculation queue from which to issue a current instruction (Column 9, Lines 42- 52), and

blocked instruction detection logic to identify instructions blocked from execution by detected blocking conditions, and to enqueue the instructions onto the recirculation queue in one of a blocked state and an unblocked state, including a respective blocking condition of each instruction within the recirculation queue, wherein instructions having a transient blocking condition are enqueued onto the recirculation queue in the unblocked state (Column 9, Lines 1-8).

20. As per claim 27-30, Claims 27-30 recite the same limitations as claims 22-25 and are rejected for the same reasons.

21. As per Claim 31, Merchant teaches: A method comprising:

Issuing an instruction selected from a queue (Column 3, Lines 25-33; Column 3, Lines 43-47);

enqueuing the instruction issued within a recirculation queue in one of a blocked state and an unblocked state if completion of the instruction is prevented by a detected blocking condition (Column 8, Lines 42-53);

resetting a state of the instruction within the recirculation queue if a detected blocking condition of at least one instruction within the recirculation queue, other than the instruction, is satisfied (Column 8, Lines 42-53); and

reissuing the instruction from the recirculation queue if a state of the instruction is indicated as the unblocked state (Column 8, Lines 42-53).

22. As per Claim 32, Merchant teaches: A method comprising:

issuing a first instruction from a queue (Column 3, Lines 25-33 and 43-47);

detecting a first blocking condition for the first instruction prior to execution of the first instruction (Column 8, Lines 12-18, also see Column 5, Lines 42-49 for other blocking conditions, such as lack of source data or waiting for memory);

setting the first instruction to one of a blocked state and an unblocked state based on the first blocking instruction (Column 8, Lines 12-18, it is blocked until the condition is cleared, or see Column 7, Lines 9-13 for unblocked instruction cases);

enqueuing the first instruction within a recirculation queue in one of the blocked state and the unblocked state if completion of the instruction is prevented by the first blocking condition (Column 8, Lines 12-18, it is put in the replay queue); and

reissuing the first instruction from the recirculation queue if the first blocking condition is satisfied (Column 8, Lines 16-18).

23. As per Claim 33, Merchant teaches: The method of claim 32 further comprising:

detecting a second blocking condition for a second instruction, wherein the second blocking condition differs from the first blocking condition and the second instruction differs from the first instruction (Column 8, Lines 12-18, if it can detect one instructions blocking condition, it can detect other instructions blocking conditions as well); and

reissuing the first instruction from the recirculation queue if the second blocking condition is satisfied (Column 11, Lines 19-21, when the "first" instruction in the queue clears its blocking condition (which could be the "second" or "first" instruction in terms of the claim language), all instructions re-issue).

24. As per Claim 34, Merchant teaches: The method of claim 32 further comprising:

setting the first instruction to an unblocked state based on the first blocking condition (Column 7, Lines 8-12); and

enqueuing the first instruction within the recirculation queue in the unblocked state until the first blocking condition is satisfied (Column 7, Lines 8-12, it will sit in the unblocked state in the queue until it can properly issue).

25. As per Claim 35, Merchant teaches: The method of claim 34 further comprising:

detecting a second blocking condition for a second instruction, wherein the second blocking condition differs from the first blocking condition and the second instruction differs from the first instruction (Column 8, Lines 12-18, if it can detect one instructions blocking condition, it can detect other instructions blocking conditions as well);

setting the second instruction to a blocked state based on the second blocking condition (Column 8, Lines 12-18, it is put in the replay queue); and

enqueuing the second instruction within the recirculation queue in the blocked state until the second blocking condition is satisfied (Column 8, Lines 16-18).

26. As per Claim 36, Merchant teaches: The method of claim 32, wherein enqueuing comprises:

determining whether the first blocking condition is a transient blocking condition (Column 7, Lines 8-12 and Column 8, Lines 12-18, it determines if it is a short or long latency event); and

setting the first instruction to the unblocked state if the first blocking condition is transient (Column 7, Lines 8-12).

Claim Rejections - 35 USC § 103

27. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

28. Claims 10 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Merchant, in view of Official Notice.

29. As per claims 10 and 20: Merchant et al. do not explicitly disclose using a circular queue. However, they do disclose using a FIFO queue (Merchant et al.: Column 9, Lines 33-36). Using a circular FIFO queue is well-known in the art since it is easier to use a circular FIFO queue than shifting each entry after each dequeue (Official Notice).

Response to Arguments

30. Examiner notes the amendments to the specification and the claims, and has withdrawn the 35 U.S.C. 101 rejection in light of the amendments.

31. Despite Applicant's amendments, and Examiners statement that they may potentially overcome Merchant upon further consideration, in light of said further consideration of the Merchant reference, in combination with the Applicant's arguments, Examiner is not yet convinced that the claims distinguish over Merchant. Applicant has argued that in Merchant, instructions are not enqueued because of a detected block condition, and are instead enqueued based on long latency events. However, Examiner considers a long latency event to be a blocking condition, and additionally, as seen in Paragraph 33 of the Applicant's own specification, Applicant defines a long latency event as a blocking condition (such as a memory latency or bandwidth bound condition, which is also defined as a long latency event, in Merchant, Column 2, Lines 53-56). Therefore, Examiner is not persuaded by the argument that a long latency event is not a blocking condition, because it does appear to be one.

Further, in regards to Claim 1, Applicant has argued that Merchant enqueues an instruction and its dependents based on a long latency event and are released when the long latency event is released, as opposed to the claim, which states that two instructions are enqueued until respective blocking conditions are satisfied. However, as discussed above, a long latency event is a blocking condition, as it prevents execution of the instruction, blocking it from execution. Additionally, upon a further search of

Merchant, in Column 11, Lines 19-26, in one embodiment, when one instruction satisfies its blocking condition, all instructions in the queue are released, thus an instruction in the replay queue would be released, based on another instructions blocking condition being satisfied, fulfilling the claim language.

Although not directly argued, in new claims 32 and 33, this concept is expanded upon in more detail, and has made clear that the first and second instructions have different blocking conditions, however, again, since Merchant can release the entire queue on the detection of one instruction fulfilling its blocking condition, Merchant appears to still read on the claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT E. FENNEMA whose telephone number is (571)272-2748. The examiner can normally be reached on Monday-Friday, 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

Robert E Fennema
Examiner
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RF